

# Interface Roughness Effects in Ultra-Thin Tunneling Oxides

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Advanced MOSFET for ULSI and novel silicon-based devices require the use of ultra-thin tunneling oxides where non-uniformity is often present. We report on our theoretical study of how tunneling properties of ultra-thin oxides are affected by roughness at the silicon/oxide interface. The effect of rough interfacial topography is accounted for by using the Planar Supercell Stack Method (PSSM) which can accurately and efficiently compute scattering properties of 3D supercell structures. Our results indicate that while interface roughness effects can be substantial in the direct tunneling regime, they are less important in the Fowler-Nordheim regime.

*Keywords:* Ultrathin, oxide, SiO<sub>2</sub>, tunneling, interface roughness

## 1. INTRODUCTION

The continued scaling of Metal-Insulator-Semiconductor (MIS) device structures has brought much attention to ultrathin oxides. Normal operation of a MOSFET with 1.5 nm direct-tunneling gate oxide has been reported [1]. Tunneling through oxide barriers, as a mechanism for leakage currents, is of particular interest. Typical theoretical analysis models the oxide layer as a 1D barrier with an effective barrier height and an effective mass. The barrier height may be obtained experimentally or treated as a fitting parameter, while the effective mass is normally

used as a parameter for fitting measured current-voltage (I-V) characteristics [2]. Tunneling coefficients can be calculated using the well-known WKB approximation. Integration of tunneling coefficient curves, with the appropriate Fermi factors describing carrier statistics, then yields an analytical I-V curve formula [3] which can be used conveniently for comparison with experimental data. A somewhat similar treatment uses multiple scattering theory instead of the WKB approximation to compute tunneling coefficients to provide clarification of mechanisms for leakage currents through ultrathin oxides [4]. A still more advanced treatment solves Poisson and Schrodinger equa-

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tions self-consistently for accumulated layers in metal-oxide-semiconductor devices to calculate tunneling currents [5].

An important aspect typically not treated in these models is oxide non-uniformity. Cundiff and co-workers [6] showed experimental evidence that roughness at the Si/SiO<sub>2</sub> interface increases with decreasing oxide layer thickness. This makes interface roughness particularly important in ultrathin oxides. Interface roughness can have dramatic effects on the current-voltage characteristics of MIS structures. It has been shown that constant current stressing of MIS structures in the Fowler-Nordheim tunneling regime can induce non-uniformities at the Si/SiO<sub>2</sub> interface [7]. This quasi-breakdown in the oxide can lead to dramatic increases in direct tunnel current. In this paper we treat the MIS tunnel structure using a 3D model which is similar to the standard models, but allows for 3D potential variations associated with Si/SiO<sub>2</sub> interfacial non-uniformity.

## 2. METHOD

Standard treatment uses a one-dimensional potential to describe the oxide barrier. With interfacial non-uniformity, we need to use a three-dimensional description. In principle, the variations in the non-uniform potential extend indefinitely in the directions along the interface. In practice, we do not perform computation for an infinite domain, but use instead a quasi-3D supercell geometry to approximate the physical problem. We treat the problem of tunneling through a non-uniform barrier using the Planar Supercell Stack Method (PSSM) [8]. The device structure treated by PSSM consists of an active layer sandwiched between two semi-infinite flat band electrode regions. Let the  $z$  axis be the direction of current flow. Then the active region is composed of a stack of  $N_z$  layers perpendicular to the  $z$ -direction, with each layer containing a periodic array of rectangular planar supercells of  $N_x \times N_y$  sites. A one-band nearest-neighbor tight-binding Hamiltonian

is used to describe the potential over this volume of interest. Our model is formally equivalent to the one-band effective mass equation.

$$-\frac{\hbar^2}{2} \nabla \cdot \frac{1}{m(\mathbf{x})} \nabla \psi + V(\mathbf{x})\psi = E\psi, \quad (1)$$

discretized over a Cartesian grid, and subject to periodic boundary conditions (with supercell periodicity) in the  $x$ - and  $y$ -directions, and open boundary conditions in the  $z$ -direction. PSSM solves the quantum mechanical scattering problem exactly for the 3D geometry described by the planar supercell stack, and allows us to compute transmission coefficients with a high degree of numerical accuracy and efficiency. Note that even though the supercell geometry imposes an artificial periodicity to make computations tractable, the use sufficiently large supercells can minimize supercell artifacts and yield excellent descriptions of the physical problem.

## 3. RESULTS AND DISCUSSION

Our model of the MOS tunnel structure consists of a metal (or poly-Si) electrode, followed by a pure oxide layer, then a rough interfacial layer, and finally a silicon electrode. We assume that the rough interfacial layer consists of a 50%–50% mixture of oxide and Si in random configurations. The Si sites, and the oxide sites, for that matter, may aggregate and form patches. We will call these silicon patches islands, and characterize them by their lateral extent (island size) and the thickness of the interfacial layer (island height). For convenience, we also assume flat-band conditions in the metal and silicon electrodes, and let all the voltage drop occur in the oxide and the rough interface. The potential barrier height and the effective mass of the oxide barrier is taken to be 3.22 eV, and  $0.35 m_0$ , respectively. We use a cubic mesh with discretization distance of 0.13575 nm, and  $64 \times 64$  planar supercells in our simulations.

Figure 1 shows transmission coefficient spectra for three MOS tunnel structures with rough Si/

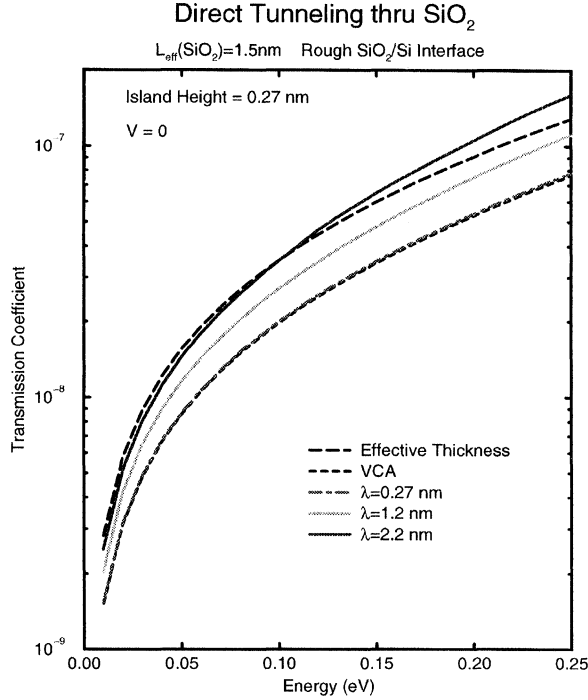


FIGURE 1 Transmission coefficient spectra for MOS tunnel structures with rough Si/SiO<sub>2</sub> interfaces characterized by different island sizes, at zero applied bias. For comparison, results for 1D models using effective barrier thickness and effective barrier height are also shown.

SiO<sub>2</sub> interfaces characterized by island sizes of  $\lambda = 0.27, 1.2$  and  $2.2$  nm. The pure oxide tunnel barrier layer is  $1.36$  nm thick, and the height of the rough interfacial layer is  $0.28$  nm. Note that tunneling probabilities increase considerably with island size. Results of two 1D models are also plotted for comparison. The first treats the oxide and the interfacial layer as having a combined effective thickness of  $1.5$  nm (the thickness of the pure oxide layer, plus half the thickness of the interfacial layer); the second treats the interfacial layer as having a potential height which is the average of the oxide and the silicon potentials (i.e., the virtual crystal approximation, or VCA potential). Note that the effective thickness model does not offer a good description of the rough interfaces. The VCA result agrees well only with that obtained for the sample with the small island size. The reason for the agreement is because when island sizes are

smaller than the deBroglie wavelength of the incoming electron, the random potential at the interface is only seen by the electron in an averaged (VCA) sense. In structures where island sizes become larger than the electron deBroglie wavelength, an electron, in a sense, finds its way through the “softer” spots (portions with lower potential, i.e., the silicon islands) of the interfacial layer, and thereby enhance its tunneling probability.

This is demonstrated in Figure 2. The top panel shows the transmission coefficient spectra of the  $\lambda = 0.27$  nm and  $\lambda = 2.2$  nm structures again for reference, while the bottom panel shows the curves of island transmission fraction, defined as the ratio of the sum of probability densities over all silicon sites in the interfacial layer divided by the total probability density in the interfacial layer. Since the interfacial layer consists of 50% silicon sites and 50% oxide sites, if an electron shows no preference for tunneling through the silicon islands

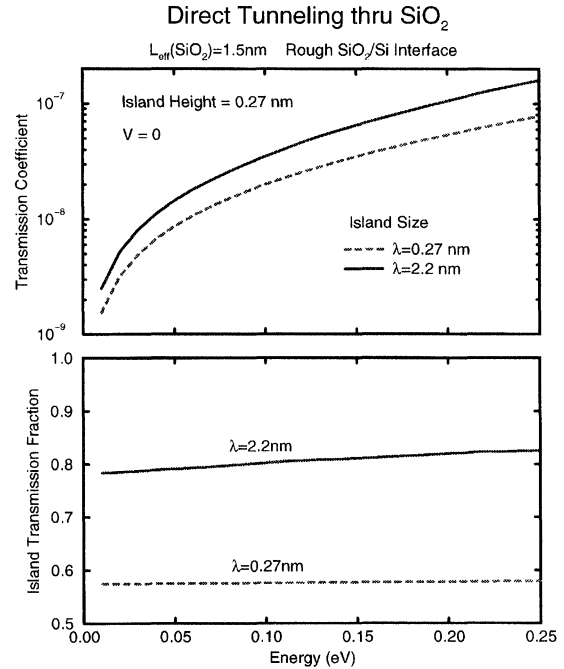


FIGURE 2 Transmission coefficients and island transmission fractions for two MOS structures with rough interfaces characterized by different island sizes, at zero applied bias.

or the oxides, the island transmission fraction would be 0.5; a fraction greater than 0.5 indicates a preference for tunneling through the silicon islands. Our results show that in the  $\lambda = 0.27$  nm (small island) structure, there are essentially no preferential pathways through the roughness layer. However, in the  $\lambda = 2.2$  nm (large island) structure, there is a definite preference for tunneling through the silicon islands. In fact, in this case the island transmission fraction increases with electron energy, or decreasing deBroglie wavelength.

We next examine the effect of interface roughness on tunneling properties under applied bias. We use the  $\lambda = 2.2$  nm structure as in the previous figures. Figure 3 shows a set of transmission coefficient spectra for this structure under various applied biases. Transmission spectra for the corresponding VCA structure are also shown for comparison. Note that while there is a considerable difference between the supercell (with interface roughness) and VCA (without) results at low biases, the difference diminishes at high biases. This indicates that the role of interface roughness becomes less

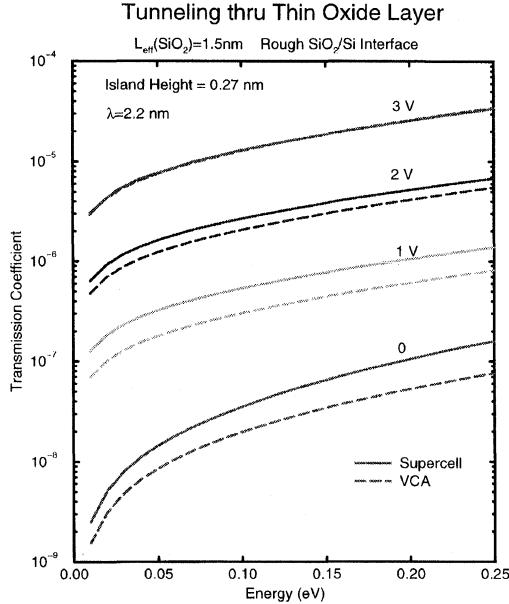


FIGURE 3 Transmission coefficient spectra for a MOS tunnel structure with rough Si/SiO<sub>2</sub> interfaces at several applied biases. Results for the corresponding VCA structure is also shown.

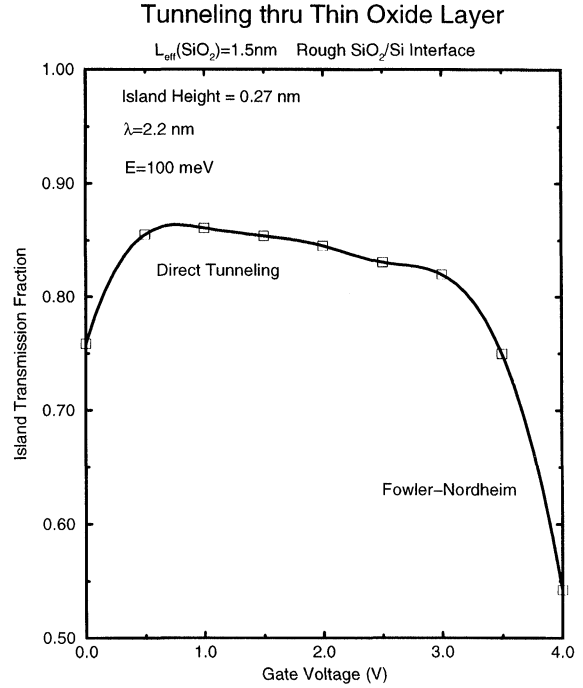


FIGURE 4 Island transmission fraction for the MOS tunnel structure depicted in Figure 3.

important as high biases. Figure 4 illustrates this further by showing the island transmission fraction for the same  $\lambda = 2.2$  nm structure as a function of applied bias. Note that while there is a preference for tunneling through silicon islands at low biases, the preference drops rapidly as the applied bias exceeds 3 volts. The reason for this turns out to be rather simple. At low biases, the device structure operates under the direct tunneling regime. An electron going through the rough interfacial layer sees the oxide portions as energy barriers and the silicon islands as open pathways. At sufficiently high biases, the device operation transitions to the Fowler-Nordheim tunneling regime, where the conduction band edge at the trailing interface of the barrier (in our case, the rough interfacial layer) is biased below the incoming electron energies. Thus the oxide portions of the rough interfacial layer no longer act as electron barriers, putting them on more equal footing with the silicon islands. In other words, in the low-bias direct tunneling

regime, an electron traverses through the oxide portions of the interfacial layer with evanescent characteristics, and the silicon portions with propagating characteristics. In the high-bias Fowler-Nordheim tunneling regime, an electron traverses through both types of the interfacial layer as a propagating state, hence there would be less reasons for preferential pathways.

In summary, we have studied tunneling through MOS structures with rough Si/SiO<sub>2</sub> interfaces using a 3D supercell simulation. We find that interfacial non-uniformities make oxides more permeable in the direct tunneling regime, especially in structures with larger islands. In the Fowler-Nordheim regime, however, non-uniformity effects on tunneling characteristics are less pronounced.

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### Authors' Biographies

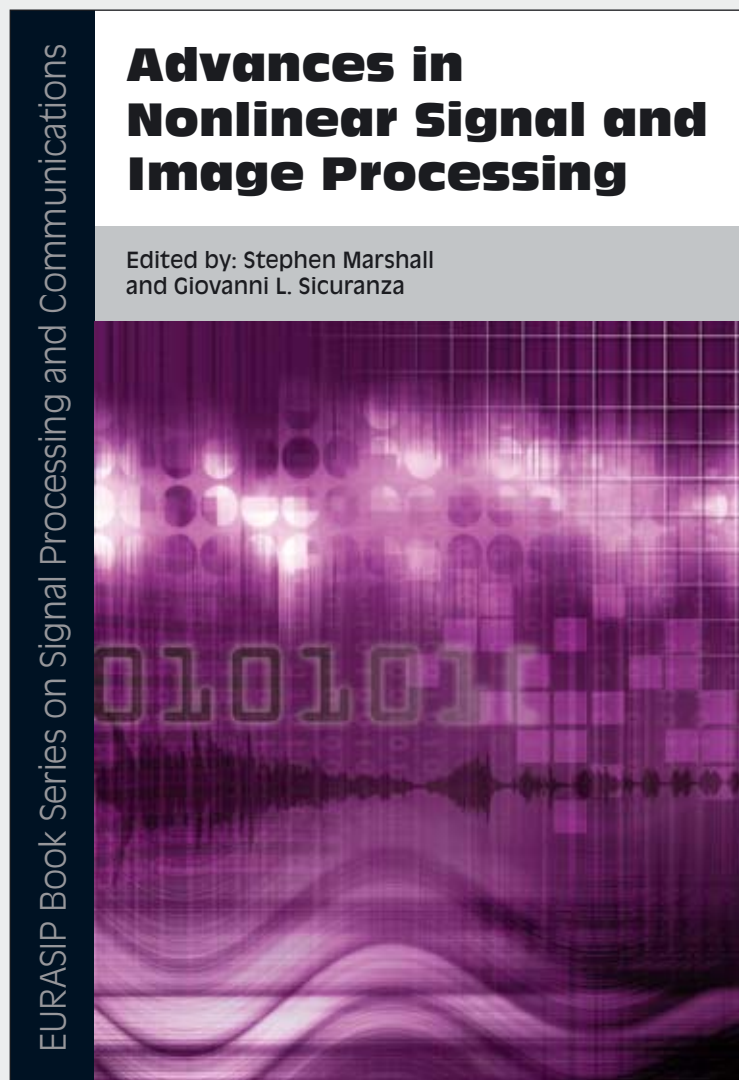
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